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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/814,392
Filing Date: March 31, 2004
Appellant(s): DYBSETTER ET AL.

Peter F. Malen Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 13, 2007 appealing from the Office action mailed January 10, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,401,176	Fadavi-Ardekani et al.	06-2002
5,893,153	Tzeng et al.	04-1999
6,275,885	Chin et al.	08-2001
5,999,299 (Evidentiary Reference)	Chan et al.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 and 9-33 are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) in view of Tzeng et al. (US 5,893,153).

As per **claims 1, 6, 9, 14, 20-22 and 28-30**, Fadavi-Ardekani discloses

"In a system/system/controller that includes"

"a system memory," as **["memory 200" (Figure 1)]**

"and a plurality of processors" **[With respect to this limitation, Fadavi-Ardekani discloses a plurality of agents that access memory "agents 100-104" (Figure 1) and "agents 100-108" (Figure 2) and explains that "each of the plurality of agents 100, 104 may be any suitable processing element, e.g., a digital signal processor (DSP), on demand transfer (ODT) engine, microprocessor or microcontroller" (Column 3, lines 46-49)]**

"and one or more other memory consumers that each access the system memory through a memory controller," **[With respect to this limitation, Fadavi-Ardekani discloses a plurality of agents that access memory "agents 100-104" (Figure 1) and "agents 100-108" (Figure 2) and explains that one of the agents can be a master process and "the other agents can be slave peripheral devices or co-processors" (Column 3, lines 50-52)]**

"a method for the memory controller to manage access to the system memory for each of the plurality of processors and the one or more other memory consumers, the method comprising the following:" as **[Fadavi-Ardekani discloses this limitation as "arbiter 102" and explains that "an arbiter and switch 102 allows one of the plurality of agents 100 or 104 o access the shared synchronous memory 200 at any one time" (Column 3, lines 53-55)]**

“an act of the memory controller allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles;” **[Fadavi-Ardekani discloses this concept as “one of the plurality of agents, e.g., agent 100 may be designated as having a higher level (i.e., a super level) with respect to the other agents, e.g. agents 104 to 108” (Column 5, lines 13-16 and Figures 1 and 2) and explains that the “super agent” is not required to arbitrate for access to memory with the other agents (Column 5, lines 30-38); therefore, the “super agent” is guaranteed access to memory during a first cycle wherein “if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might be used by the super agent A to access the shared synchronous memory” (Column 7, lines 7-10 and Figures 2 and 4)]**

“and an act of the memory controller allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles” **[Fadavi-Ardekani discloses this concept as “non-super agents arbitrate for ownership and access to the shared synchronous memory 200 during open windows of time, either between accesses by a super agent or the interim during an extended access by the super agent A” (Column 6, lines 60-64) and provides an example in which “if a cycle extension of a memory**

request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13). It is also taught that "non-super agents" arbitrate for access to memory on a "first-come, first-served bases, on a priority basis, or other suitable decisive decision criteria by the arbiter and switch 202. For instance, the winning non-super agent may be provided time division multiplexed access to the shared synchronous memory" (Column 6, lines 1-8) wherein agents can be processors or other peripheral devices (Column 3, lines 49-52); therefore, processors and peripheral devices arbitrate/compete for memory access during a second memory access cycle, and access might be granted to a processor on a conditional basis].

Fadavi-Ardekani does not disclose expressly that during the arbitration cycle, a processor is given access to memory "subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory."

Tzeng discloses the concept of during an arbitration cycle, giving access to memory to a processor "subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" as **["when an instruction from the core logic unit and a DMA request from an external input/output unit are simultaneously present at the external cache**

controller, the integrated input/output system maintains data coherency by implementing a rule of procedure that prioritizes the DMA request over the core logic unit instruction" (Column 2, lines 37-42); therefore, when there are not I/O unit requests to access memory, access by the processor/logic unit/cpu will be imposed (*as claimed in claim 6*); otherwise, I/O units (*other memory consumers*) will be allowed to access memory (*as claimed in claim 9*)]; therefore, a memory consumer is allowed to access memory during "regardless of having received the request from the second processor to access the system memory during the second division of the second memory access cycle" as (*as in claim 14*) **[DMA accesses are prioritized (Column 2, lines 37-42)]**.

Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access control method/system; which during a second memory access cycle, arbitrates access to memory by multiple agents which may be processors or other peripheral devices based on priority as taught by Fadavi-Ardekani and further give higher priority to peripheral or I/O devices over processors or core logic units as taught by Tzeng.

The motivation for doing so would have been because Tzeng discloses that during an arbitration cycle, access to memory to a processor should be given "subject to a determination that at least one of the one or more other memory consumers has not

also requested access to the system memory" because **["Many external I/O devices operate in real time. Moving DMA instructions ahead of instructions from the core logic unit has the added benefit of ensuring that the external I/O devices properly operate in such a real time environment" (Column 2, lines 53-57)]**.

Therefore, it would have been obvious to combine Tzeng et al. (US 5,893,153) with Fadavi-Ardekani et al. (US 6,401,176) for the benefit of creating a method of controlling memory accesses by multiple units to obtain the invention as specified in claims 1, 20-22 and 28-30.

As per **claims 2-5 and 10-13**, the combination of Fadavi-Ardekani and Tzeng discloses "A method in accordance with claims 1 and 9," **[See rejection to claims 1 and 9 above]** "wherein the first division in a given memory access cycle of the plurality of memory access cycles is before/after/adjacent in time/separated in time with the second division in the given memory access cycle" **[Fadavi-Ardekani discloses these limitations as memory access to a super agent (*first processor, as claimed*) is given without having to arbitrate with non-super agents (*second processors or other memory customers devices as claimed*) (Column 5, lines 35-38) wherein "non-super agents" arbitrate for memory access during open windows; for example, "if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super**

agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13). Fadavi-Ardekani also discloses; "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67); therefore, a super-agent memory access cycle *(or first cycle, as claimed)* may be before/after/adjacent in time/separated in time from a memory access by a non-super agent (*second processors or other memory customers devices as claimed*)].

As per **claims 15, 23 and 31**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system/controller in accordance with claims 1, 20 and 28," **[See rejection to claims 1, 20 and 28 above]** "further comprising the following:"
"an act of the memory controller allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles" **[This claim is rejected for the same reasons as noted above for the rejection to claim 1. Additionally, Fadavi-Ardekani discloses that "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67) and explains that one or more super agents might exist (Column 6, lines**

66-67); therefore, super-agent memory access cycles can occur at any time with higher/guaranteed priority].

As per **claims 16-17, 24-25 and 32-33**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system/controller in accordance with claims 1, 15, 20, 23, 28 and 31" **[See rejection to claims 1, 15, 20, 23, 28 and 31 above]** "further comprising the following:"

"an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" **[This claim is rejected for the same reasons as noted above for the rejection to claim 1. Additionally, Fadavi-Ardekani discloses that "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67) and explains that one or more super agents might exist (Column 6, lines 66-67); therefore, super-agent memory access cycles can occur at any time with higher/guaranteed priority]**.

As per **claims 18 and 26**, the combination of Fadavi-Ardekani and Tzeng discloses “A method/system in accordance with claims 1 and 20,” **[See rejection to claims 1 and 20 above]** “wherein at least one of the one or more other memory consumers includes a serial interface” **[With respect to this limitation, Fadavi-Ardekani discloses “agents can be slave peripheral devices” (Column 3, lines 51-52 and Figure 2). Tzeng also discloses (*memory consumers as claimed*) as “I/O devices 54, 55” (Figure 2). These peripheral or I/O devices might be modem, keyboard or serial printers, which are well known serial devices]**.

As per **claims 19 and 27**, the combination of Fadavi-Ardekani and Tzeng discloses “A method/system in accordance with claims 1 and 20,” **[See rejection to claims 1 and 20 above]** “wherein the one or more memory consumers comprise a plurality of memory consumers” **[With respect to this limitation, Fadavi-Ardekani discloses multiple agents accessing memory and explains that “agents can be slave peripheral devices” (Column 3, lines 51-52 and Figure 2). Tzeng also discloses “I/O devices 54, 55” (Figure 2)]**.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 6 above, and further in view of Chin et al. (US 6,275,885).

As per **claims 7-8**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system in accordance with claim 6," **[See rejection to claim 6 above]** but does not disclose expressly that **"**the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:" a request "is not issued by the second processor if the at least one of the one or more memory consumers had requested access" or "request from the second processor is not received by the memory controller if the at least one of the one or more memory consumers had requested access."

Chin discloses a memory access control method/system in which "a request is not issued by the second processor if the at least one of the one or more memory consumers had requested access" or "the request from the second processor is not received by the memory controller if the at least one of the one or more memory consumers had requested access" as **["a bus interface unit includes a memory arbiter which grants ownership of the memory bus to a peripheral device cycle rather than a concurrent CPU cycle when certain conditions exist. The bus interface unit therefore involves a mechanism for stalling CPU cycles on the CPU bus until after the peripheral device obtains mastership of the memory bus. In this fashion, the memory arbiter will grant mastership to a peripheral cycle since a CPU derived cycle is prevented from reaching the memory arbiter" (Column 3, lines 7-17) and explains that "upon receiving the priority bus request signal form the bus interface unit, each and every CPU linked to the CPU bus is stalled from**

sending address and data across the CPU bus" (Column 3, lines 29-32) wherein "by asserting a signal (BNR#) any agent can prevent the current CPU bus owner from issuing new transactions" (Column 9, lines 38-41)].

Fadavi-Ardekani et al. (US 6,401,176), Tzeng et al. (US 5,893,153) and Chin et al. (US 6,275,885) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access control method/system; which during a second memory access cycle, arbitrates access to memory by multiple agents which may be processors or other peripheral devices based on priority as taught by Fadavi-Ardekani, give higher priority to peripheral or I/O devices over processors or core logic units as taught by Tzeng and further having stalling CPUs from issuing memory access requests or not receiving memory access request by a memory arbiter as taught by Chin.

The motivation for doing so would have been because Chin discloses that CPUs are stalled from issuing memory access requests or these memory access requests are not received by a memory arbiter to **[keep memory coherent and "assure that peripheral-derived data is written into the system memory before that data is read by the CPU" (Column 2, lines 64-60) as peripheral-derived data processing is time critical or real-time (Tzeng; Column 2, lines 53-57)]**.

Therefore, it would have been obvious to combine Chin et al. (US 6,275,885) with Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) for the

benefit of creating a method of controlling memory accesses by multiple units to obtain the invention as specified in claims 7-8.

Claims 34 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 28 above and further in view of Chan et al. (US 5,999,299), used as evidentiary reference.

It is noted that the combination of Fadavi-Ardekani and Tzeng does not disclose a memory controller is implemented in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver. However, the examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the controller as being claimed in claim 28 in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver, since it is well known in the art that a laser transceiver comprises a memory and a controller as evidenced by **[Chan et al. US 5,999,299 (Figure 4 and related text); which discloses a laser transceiver wherein access to a memory is controlled by controller]**. A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim form the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)).

Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 34 above and further in view of Chan et al. (US 5,999,299), used as evidentiary reference.

The combination of Fadavi-Ardekani and Tzeng does not disclose expressly that a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to apply the controller of claim 34 (Refer to the rejection of claim 34 above) to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G. Applicant has not disclosed that applying the controller of claim 34 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any memory size and any transceiver bandwidth size [**Refer to Chan et al. US 5,999,299 (Col. 1, lines 60-67), which disclose laser transceivers having different transfer rates/bandwidths; thereby, rendering different transfer rates/bandwidths of a transceiver as a characteristic of a laser transceiver that is well known in the art]** because the combination Fadavi-Ardekani and Tzeng provides a method/system/controller to control accesses to memory by a plurality of processors and other peripheral or I/O devices, regardless of the size of the memory and Fadavi-Ardekani explains that **["the principles of the present invention relate equally to all types of synchronous memory" (Column 3, lines 44-45)]**. Furthermore, Examiner

states that “at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to apply the controller of claim 34 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G;” Applicant should note that such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose,* 105 USPQ 237 (CCPA 1955).

Therefore, it would have been obvious to one of ordinary skill in this art to modify the combination of Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) to obtain the invention as specified in claims 35-39.

(10) Response to Argument

A. § 103(a) rejection of claims 1-6 and 9-33 over Fadavi-Ardekani in view of Tzeng

Claims 1, 20 and 28

Appellant argues that the combination of Fadavi-Ardekani and Tzeng does not teach that ““each of a plurality of memory access cycles" be divided into at least “a first division” and "a second division" with memory access during the first division of a memory access cycle being “guaranteed” to a first processor and memory access during the second division of the same memory access cycle being “conditionally granted” to a second processor, ” as required by claims 1, 20 and 28.

In response to Appellant’s arguments, these arguments were fully considered but were not deemed persuasive.

Examiner respectfully submits that the combination of Fadavi-Ardekani and Tzeng discloses

> “an act of the memory controller allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles; and an act of the memory controller allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles” as **[“one of the plurality of agents, e.g., agent 100 may be designated as having a higher level (i.e., a super level) with respect to the other agents, e.g. agents 104 to 108 (*which corresponds to a first processor, as claimed*)” (Column 5, lines 13-16 and Figures 1 and 2) and explains that the “super agent” is not required to arbitrate for access to memory with the other agents (Column 5, lines 30-38) wherein “non-super agents (*which correspond to a second processor, as claimed*) arbitrate for ownership and access to the shared synchronous memory 200 during open windows of time, either between accesses by a super agent or the interim during an extended access by the super agent A (*which comprise conditions in order to grant access to a non-super agent; thereby conditionally granting access to a non-super agent*)” (Column 6, lines 60-64) and provides an example in which “if a cycle extension of a memory request from the super agent A lasts for N cycles (*wherein each cycle taught by Fadavi-Ardekani corresponds to a division of a plurality of memory access cycles as claimed*), the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-**

super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13); therefore, the "super agent" is guaranteed access to memory during a first cycle and "non-super agents" arbitrate for access to memory on a "first-come, first-served basis, on a priority basis, or other suitable decisive decision criteria by the arbiter and switch 202. For instance, the winning non-super agent may be provided time division multiplexed access to the shared synchronous memory" (Column 6, lines 1-8) wherein agents can be processors or other peripheral devices (Column 3, lines 49-52); therefore, processors and peripheral devices arbitrate/compete for memory access during a second memory access cycle, and access is granted to a processor on a conditional basis which comprises the condition that the super-agent is not accessing memory or has accessed memory for an extended time period].

Appellant argues that since "Fadavi-Ardekani teaches that a super agent can access memory "<u>whenever requested;</u>" therefore failing to conditionally grant memory access to a non-super agent during the second division of a plurality of memory access cycles.

This argument has been fully considered but it is not deemed persuasive.

First, the Examiner would like to respectfully point out that it appears that Appellant is misconstruing the rejection to the claims and has ignored the fact that a non-super agent or second processor accesses memory during open windows which not only exist when the super-agent or first processor is not accessing memory, but also when the super-agent has extended access lasting more than a single memory clock cycle/first division of a plurality of memory access cycles **[Refer to Fadavi-Ardekani (Col. 6, lines 20-39 and 44-49; Col. 8, lines 20-24)]**; therefore, as Fadavi-Ardekani

discloses granting access to a non-super agent during an open-window, it is disclosed conditionally granting access to a second processor or non-super agent during a second division of a plurality of memory access cycles.

Appellant should note that the claims require conditionally granting memory access to a second processor or non-super agent during the second division of a plurality of memory access cycles; therefore, when memory is granted to a non-super agent during an open window which Fadavi-Ardekani describes as **["if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13)]**; memory is conditionally granted to a non-super agent during a second division of a plurality of memory access cycles under the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle. Furthermore, even as Fadavi-Ardekani discloses super agent can access memory whenever requested; there is no requirement in the claims preventing super-agent from doing so, since the claims expressly require that access to a non-super agent or second processor be granted conditionally; therefore, it is irrelevant whether the first processor is able to take over a memory access that was granted to a second processor or non-super agent during a second division of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agent or second processor, as required by the claims.

Appellant remarks the Fadavi-Ardekani teaches away from having an allotted "second division of each of a plurality of memory access cycles" for non-super agents because such an allotted portion of each memory access cycle for non-super agents would prevent the super agent from gaining memory access whenever requested; this remark has been fully considered but it is not persuasive.

It appears that Appellant is misconstruing the rejection to the claims since Fadavi Ardekani clearly discloses that a non-super agent or second processor accesses memory during open windows which not only exist when the super-agent or first processor is not accessing memory, but also when the super-agent has extended access lasting more than a single memory clock cycle/first division of a plurality of memory access cycles **[Refer to Fadavi-Ardekani (Col. 6, lines 20-39 and 44-49; Col. 8, lines 20-24)]**; therefore, as Fadavi-Ardekani discloses granting access to a non-super agent during an open-window, it is disclosed conditionally granting access to a second processor or non-super agent during a second division of a plurality of memory access cycles.

Fadavi-Ardekani clearly teaches **["if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13)]**; therefore, memory is conditionally granted to a non-

super agent during a second division of a plurality of memory access cycles under the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle. Furthermore, even as Fadavi-Ardekani discloses super agent can access memory whenever requested; there is no requirement in the claims preventing super-agent from doing so, since the claims expressly require that access to a non-super agent or second processor be granted conditionally; therefore, it is irrelevant whether first processor is able to take over a memory access that was granted to a second processor or non-super agent during a second division of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agent or second processor, as required by the claims.

Furthermore, the Examiner would also like to point out that the reference to Fadavi-Ardekani does not teach away from the claimed invention as Fadavi-Ardekani's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton,* 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123.

Claims 2-5

Appellant's arguments with respect to claims 2-5 parallel those presented with respect to claims 1, 20 and 28. Accordingly, these arguments are addressed at least in the manner that claims 1, 20 and 28 have been addressed above.

Claims 16, 17, 24-25 and 32-33

Appellant argues that Fadavi-Ardekani does not disclose that each of a plurality of memory access cycles be divided into at least a first division, a second division and a fourth division with memory access during the first division being guaranteed to a first processor and memory access during the second and fourth divisions being conditionally granted to a second processor and a fourth processor, respectively as required by claims 16, 17, 24, and 32 and also argues that Fadavi-Ardekani does not disclose that each of a plurality of memory access cycles be divided into at least a first division, a second division and a third division with memory access during the first division being guaranteed to a first processor and memory access during the second and third divisions being conditionally granted to a second processor and a third processors, respectively as required by claims 25 and 33.

These arguments have been fully considered but they are not deemed persuasive.

> Fadavi-Ardekani discloses a plurality of memory access cycles be divided into at least a first division, a second division and a fourth division with memory access during the first division being guaranteed to a first processor and memory access during the second and fourth divisions being conditionally granted to a second processor and a fourth processor, respectively and each of a plurality of memory access cycles be divided into at least a first division, a second division and a third division with memory access during the first division being guaranteed to a first processor and memory access during the second and third divisions being conditionally granted to a second processor and a third processors, respectively as **["one of the plurality of agents, e.g., agent 100 may be designated as having a higher level (i.e., a super level) with respect to the**

other agents, e.g. agents 104 to 108 (*which corresponds to a first processor, as claimed*)" (Column 5, lines 13-16 and Figures 1 and 2) and explains that the "super agent" is not required to arbitrate for access to memory with the other agents (Column 5, lines 30-38) wherein "non-super agents (*which correspond to a second, third and fourth processors, as claimed*) arbitrate for ownership and access to the shared synchronous memory 200 during open windows of time, either between accesses by a super agent or the interim during an extended access by the super agent A (*which comprise conditions in order to grant access to non-super agents; thereby conditionally granting access to non-super agents*)" (Column 6, lines 60-64) and provides an example in which "if a cycle extension of a memory request from the super agent A lasts for N cycles (*wherein each cycle taught by Fadavi-Ardekani corresponds to a division of a plurality of memory access cycles*), the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles (*which correspond to second, third and fourth divisions of a plurality of memory access cycles*) of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B (*which correspond to a second, third and fourth processors*)" (Figures 2 and 4 and Column 7, lines 7-13); therefore, the "super agent" is guaranteed access to memory during a first cycle and "non-super agents" arbitrate for access to memory on a "first-come, first-served basis, on a priority basis, or other suitable decisive decision criteria by the arbiter and switch 202. For instance, the winning non-super agent may be provided time division multiplexed access to the shared synchronous memory" (Column 6, lines 1-8) wherein agents can be processors or other peripheral devices (Column 3, lines 49-52); therefore, processors and peripheral devices arbitrate/compete for memory access during second, third and fourth memory access cycle, and access is granted to a processor on a

conditional basis which comprises the condition that the super-agent is not accessing memory or has accessed memory for an extended time period].

Appellant should note that the claims require <u>conditionally</u> granting memory access to a second, third or fourth processors or non-super agents during second, third, or fourth divisions of a plurality of memory access cycles; therefore, when memory is granted to a non-super agent during an open window which Fadavi-Ardekani describes as **["if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13)]**; memory is conditionally granted to non-super agents during second, third or fourth divisions of a plurality of memory access cycles under the condition that a super-agent is not accessing memory or has accessed memory for more than one cycle. Furthermore, even as Fadavi-Ardekani discloses super agent can access memory whenever requested; there is no requirement in the claims preventing super-agent from doing so, since the claims expressly require that access to non-super agents or second, third and fourth processors be granted <u>conditionally</u>; therefore, it is irrelevant whether first processor is able to take over a memory access that was granted to a second, third or fourth processors or non-super agents during a second, third or fourth divisions of a plurality of memory access cycles, since this access was only conditionally granted to the non-super agents or second, third and fourth processor, as required by the claims.

Furthermore, the Examiner would also like to point out that the reference to Fadavi-Ardekani does not teach away from the claimed invention as argued by Appellant since Fadavi-Ardekani's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton,* 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123.

Claims 6, 9-14, 18-19, 21-23, 26, 27 and 29-31

Appellant's arguments directed to the rejections of claims 6, 9-14, 18-19, 21-23, 26, 27 and 29-31 on pages 17-18 reiterate the deficiencies Appellant made in the rejection of independent claims 1, 20 and 28 and do not address any new points. Therefore, examiner submits that if the rejection of the independent claims is deemed proper, the rejection of claims 6, 9-14, 18-19, 21-23, 26, 27 and 29-31 should be upheld.

Appellant remarks that the Examiner has failed to establish that there is a reasonable expectation of success in implementing the combination of Fadavi-Ardekani and Tzeng; however, the Examiner respectfully disagrees and would like to point that the combination of Fadavi-Ardekani and Tzeng discloses all the limitations required by the claims as explained above.

In response to Applicant's argument that there is not suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Fadavi-Ardekani and Tzeng are directed to and involved in memory access and control; more specifically, shared memory access and control and disclose all the limitations required by the claims [See ground of rejection above].

B. § 103(a) rejection of claims 7-8 over Fadavi-Ardekani in view of Tzeng and Chin

Appellant remarks that the Examiner has failed to establish that there is a reasonable expectation of success in implementing the combination of Fadavi-Ardekani, Tzeng and Chin; however, the Examiner respectfully disagrees and would like to point that the combination of Fadavi-Ardekani, Tzeng and Chin discloses all the limitations required by the claims as explained above.

In response to Applicant's argument that there is not suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Fadavi-Ardekani,

Tzeng and Chin are directed to and involved in memory access and control; more specifically, shared memory access and control and disclose all the limitations required by the claims [See grounds of rejection above].

C. § 103(a) rejection of claims 34 and 40-42 over Fadavi-Ardekani in view of Tzeng and further in view of assertions that it would have been obvious to user the controller as claimed in these claims

In response to Appellant's remarks that claims 34 and 40-42 do not simply recite the manner in which a claim is intended to be used, rather require that the memory controller is implemented in a laser transmitter/receiver; the Examiner would like to respectfully point out that the combination of Fadavi-Ardekani and Tzeng discloses a "memory controller… operated in a system that includes a system memory" as required by independent claim 28; which discloses applicant's invention, but does not expressly disclose that this controller is implemented in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver.

However, claims 34 and 40-42 refer to some of the many possible environments where applicant's invention could be implemented or used; therefore, it would have been obvious to one of ordinary skill in the art to use/implement applicant's invention in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver or any other environment which requires a "memory controller… operated in a system that includes a system

memory;" since it is well known in the art that a laser transmitter/receiver comprises a memory controller and a system memory; as evidenced by **[Chan et al. US 5,999,299 (Figure 4 and related text); which discloses a laser transceiver wherein access to a memory is controlled by controller]**. Furthermore, a recitation directed to the manner in which a claim is intended to be used/implemented does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)).

D. § 103(a) rejection of claims 35-39 over Fadavi-Ardekani in view of Tzeng and further in view of assertions that it would have been obvious to apply the memory controller as claimed in these claims to a laser transmitter/receiver of 1G, 2G, 4G, 10G, or greater than 10 G

In response to Applicant's remark that the combination of Fadavi-Ardekani and Tzeng do not disclose a laser transmitter/receiver that is 1G, 2G, 4G, 10G or greater than 10G ; the Examiner would like to respectfully point out that claims 35-39 refer to different characteristics of some of the many possible environments where applicant's invention could be implemented or used, further limiting claim 34 to recite that the present invention is implemented in a laser transmitter/receiver of 1G, 2G, 4G, 10G, or greater than 10 G.

It would have been obvious to one of ordinary skill in the art to use/implement the a memory controller in a transmitter/receiver having a bandwidth size of 1G, 2G, 4G, 10G, or greater than 10 G. Refer to **[Chan et al. US 5,999,299 (Col. 1, lines 60-67)]**,

which discloses laser transceivers having different transfer rates/bandwidths; thereby, rendering different transfer rates/bandwidths of transceiver as a characteristic of a laser transceiver that is well known in the art. Furthermore, claims 35-39 involve a mere change in bandwidth size of the transmitter/receiver claimed in claim 34. Applicant should note that such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose,* 105 USPQ 237 (CCPA 1955).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Yaima Campos/

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Conferees:

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